Helmholtz - OCPC - Programme 2017-2021
for the Involvement of Postdocs in Bilateral Collaboration Projects with China

PART A

Title of the project:
Design of Reliable Next Generation Computing Platforms using Emerging non-volatile Resistive Memories

Helmholtz Centre and institute:
Karlsruhe Institute of Technology (KIT) - Institute of Computer Engineering (ITEC), Chair of Dependable Nano Computing (CDNC)

Project leader:
Professor Dr. Mehdi Tahoori

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Description of the project (max. 1 page)**:**

These heterogeneous computing systems are based on the von Neumann (VN) architectures and rely on many parallel (mini-)cores with a shared SRAM cache (parallel CPUs, GPUs, SIMD-VLIWs, and vector processors). It is well recognized that these solutions suffer from major limitations such as decreased performance acceleration per core, increased power consumption, and limited system scalability. These limitations are mainly caused by the processor-memory bottleneck. Moreover, today's computers are manufactured using the traditional CMOS technology, which is reaching the inherent physical limits due to transistor down-scaling. Ultra-scaled technology nodes are suffering from high static power consumption, reduced performance gain, reduced reliability, complex manufacturing process leading to low yield and complex testing process, and extremely costly masks. On the other hand, today's emerging applications (such as Internet-of-Things and Big Data analytics) are posing serious challenges on current computer architectures and technologies. More computing power and efficiency is required at lower power/energy, with important constraints imposed on sizing, reliability, security, etc. Therefore, there is an urgent need to explore alternative architectures in the light of emerging non-volatile technologies, not only to further increase the computing efficiency at a lower cost, but also to further reduce the overall energy.

Computing In Memory is an emerging concept based on the tight integration of traditionally separated memory elements and combinational circuits, allowing minimizing time and energy

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needed to move data across digital architectures. In the current digital von Neumann architectures, data are transferred back and forth between the memory and the computing unit, thus making them slower and power hungry. The most promising solutions for in-memory computing architectures are based on the use of emerging technologies, such as resistive or magneto-resistive devices, that are able to act as both storage and information processing units. Despite the promising nature of the in-memory computing based architectures built with emerging devices, many issues related to the devices themselves and to their double use (storage and computing unit) have still to be solved. Modeling and characterization of fabrication defects, variability and reliability issues, fault analysis and modeling are still lacking maturity, as consequence of novel fabrication processes and variety of design proposals. These issues explain the limitations of the existing test solutions for emerging memory arrays and the lack of test strategies for in-memory computing structures thus motivating our research focus in this direction.

This project aims at providing techniques for design, high quality test and reliability of emerging computing paradigms such as Compute-in-Memory (CIM) and neuromorphic computing circuits and architectures based on emerging resistive memory technologies, such as spintronic (STT, SOT) and memristive devices (ReRAM, OxRAM, PCM). In order to achieve this goal, the project will focus on the development of novel circuit designs and architectures, fault models, reliability improvement, characterization and test methods targeting at enhancing the dependability of the spintronic-based computing applications.

Description of existing or sought Chinese collaboration partner institute (max. half page)**:**

The research group at KIT-CDNC, headed by Prof. Tahoori, and Beihang University in Beijing, headed by Prof. Weisheng Zhao are internationally well-known in the area of spintronics with complementary expertise and background. They have had several mutual interests in the topic of spintronics, while the main focus of the Prof. Zhao's team is on device and circuit level aspects, the group of Prof. Tahoori at KIT is more focused on higher level aspects such as architecture and system as well as test and reliability solutions. The two groups have organized together a special session on spintronic memories at DATE conference and Prof. Tahoori has made a visit to Beihang university earlier this year in which he made a seminar presentation and we had several discussions to explore collaboration opportunities. This postdoc program, in which a graduating PhD student of Prof. Zhao will be planned to visit and stay at KIT will strengthen the ongoing collaboration and long-term activities.

Required qualification of the post-doc:

- **PhD in Microelectronics, electrical engineering or computer engineering**
- **Experience with device modelling, circuit design and simulation of Spintronics (STT or SOT) and/or memristive devices**
- **Additional skills in circuit design, reliability modelling, EDA tools**

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PART B

Documents to be provided by the post-doc, necessary for an application to OCPC via a postdoc-station in China, which is affiliated to a research institution like a university:

- Detailed description of the interest in joining the project (motivation letter)
- Curriculum vitae, copies of degrees
- List of publications
- 2 letters of recommendation
- Proof of command of English language

PART C

Additional requirements to be fulfilled by the post-doc:

- Max. age of 35 years
- PhD degree not older than 5 years
- Very good command of the English language
- Strong ability to work independently and in a team

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